Approval: 9th Senate Meeting

Course Name: Mixed Signal VLSI Design

Course number: EE 619

Credit: 3-0-2-4 (L-T-P-C)

Prerequisite: EE 512 CMOS Analog IC design

Students intended for: UG/PG

Elective or Core: Elective

Semester: Even/Odd

Preamble: This course builds the advanced CMOS analog IC design. The course is intended to teach undergraduate and graduate students. This course focuses on the concepts of mixed signal VLSI design. The course will give practical aspect of mixed signal VLSI blocks such as comparators, data converters, oscillators and phase locked loop. As a part of this course, the students will use industry standard softwares and tools such as Cadence's Virtuoso schematic, Spectre simulator and Mentor Graphics' Eldo and Calibre for post layout simulations along with the parasitic extractions. The design problems given in the form of assignments will be designed and simulated in a standard CMOS technology by students. The study will cover design issues on the PVT variations and statistical mismatches in temperature and process (MonteCarlo). In summary, the course is designed with considering the need of VLSI design industry.

Course objective: The course aims to teach advance design techniques for bandgap references, comparators, ADC/DAC, oscillators and PLL. The objective of the course is to design and to implement the product level design blocks for VLSI applications.

Course Content:

Sample and hold and trans-linear circuits [2 hours]

1. Performance of sample-and-hold circuits – testing sample and holds, MOS sample-and-hold basics, examples of CMOS S/H Circuits, bipolar and BiCMOS Sample-and-Holds, Trans-linear gain Cell, trans-linear multiplier

Switched Capacitor circuits [4 hours]

1. Basic building blocks – opamps, capacitors, switches, non-overlapping clocks, Basic operation and analysis of switched capacitor circuits, resistor equivalence of a switched capacitor, parasitic-sensitive integrator, parasitic-insensitive integrators, signal-flow-graph analysis, noise in switched-capacitor circuits
2. First-Order Filters – switch sharing, fully differential filters, biquad filters, low-Q biquad filter, high-Q biquad filter, Charge injection, switched-capacitor gain circuits, parallel resistor-capacitor circuit, resettable gain circuit, capacitive-reset gain circuit, correlated double-sampling techniques, other switched-capacitor circuits viz. amplitude modulator, full-wave rectifier, peak detectors, voltage-controlled oscillator, sinusoidal oscillator

Comparators [3 hours]

- Comparator specifications – input offset and noise, hysteresis

- Opamp as a comparator – input-offset voltage errors, charge-injection errors, making charge-injection signal independent, minimizing errors due to charge-injection, speed of multi-stage comparators
- Latched comparators, latch-mode time constant, latch offset, examples of CMOS and BiCMOS comparators, input-transistor charge trapping

Data converters specifications [2 hours]

3. Ideal D/A converter, ideal A/D converter, quantization noise, deterministic approach, stochastic approach, signed codes, performance limitations, resolution, offset and gain error, accuracy and linearity

Nyquist rate digital-to-analog converters (DAC) [4 hours]

- Decoder-based converters – resistor string converters, folded resistor-string converters, multiple resistor-string converters, signed outputs,
- Binary-scaled converters – binary-weighted resistor converters, reduced-resistance-ratio ladders, R-2R-based converters, charge-redistribution switched-capacitor converters, current-mode converters, glitches
- Thermometer-code converters – thermometer-code current-mode D/A converters, single-supply positive-output converters, dynamically matched current sources
- Hybrid converters – resistor-capacitor hybrid converters, segmented converters

Nyquist rate analog-to-digital converters (ADC) [12 hours]

- Introduction to integrating converters, flash converters, issues in designing flash ADC,
- Successive-approximation converters – DAC-based successive approximation, charge-redistribution A/D, resistor-capacitor hybrid, speed estimate for charge redistribution converters, error correction in successive-approximation converters, multi-bit successive-approximation
- Algorithmic (or cyclic) A/D Converter – ratio-independent algorithmic converter,
- Pipelined A/D converters – one-bit-per-stage pipelined converter, 1.5 bit per stage pipelined converter, pipelined converter circuits, generalized k-bit-per-stage pipelined converters
- Two-step A/D converters, two-step converter with digital error correction,
- Interpolating A/D converters, folding A/D converters, time-interleaved A/D converters

Oversampling ADCs [8 hours]

- Oversampling without noise shaping, quantization noise modeling, white noise assumption, oversampling advantage, the advantage of 1-bit D/A converters
- Oversampling with noise shaping, noise-shaped delta-sigma modulator, first-order noise shaping, switched-capacitor realization of a first-order A/D converter, second-order noise shaping, noise transfer-function curves, quantization noise power of 1-bit modulators, error-feedback structure
- System architectures – system architecture of delta-sigma A/D converters, system architecture of delta-sigma D/A converters,
- Digital decimation filters – multi-stage, single stage, higher-order modulators – interpolative architecture, multi-stage noise shaping (MASH) architecture, bandpass oversampling converters, Practical considerations – stability, linearity of two-level converters, idle tones, dithering, opamp gain,
- Multi-bit oversampling converters – dynamic element matching, dynamically matched current

source D/A converters, digital calibration A/D converter, A/D With both multi-bit and single-bit feedback

Phase locked loop **[6 hours]**

- Basic phase-locked loop architecture, voltage controlled oscillator, divider, phase detector, loop filer, the PLL in lock,
- Linearized small-signal analysis – second-order PLL model, limitations of the second-order small-signal model, PLL design example
- Jitter and phase noise – period jitter, P-cycle jitter, adjacent period jitter, other spectral representations of jitter, probability density function of jitter
- Electronic oscillators – ring oscillators, LC oscillators, phase noise of oscillators, jitter and phase noise in PLLS, input phase noise and divider phase noise, VCO phase noise, loop filter noise

Text book:

1. "Analog Integrated Circuit Design" by Tony Chan Carusone, David A. Johns, Kenneth W. Martin, second edition, 2012, Wiley

Reference books:

2. "CMOS Analog Circuit Design" by Phillip Allen and Douglas R. Holberg., second edition, Oxford university press, 2002
3. "Analog Design Essentials" by Willy M. C. Sansen, Springer, 2006
4. "Design of Analog CMOS Integrated Circuits" by Behzad Razavi, McGraw Hill, 2001